What is claimed is:

1. A hetero field effect transistor comprising:

a substrate;

a channel layer provided on the substrate with a buffer layer disposed between the substrate and the channel layer;

a spacer layer constituted by a semiconductor having a band gap larger than a band gap of the channel layer, the spacer layer being formed to hetero-join to the channel layer; and

a carrier supply layer formed to be adjacent to the spacer layer, wherein

the substrate is made of InP,

the channel layer comprises a compound semiconductor layer represented by a formula $Ga_xIn_{1-x}N_yA_{1-y}$ in which A is As or Sb, composition x satisfies $0 \leqq x \leqq 0.2$, and composition y satisfies $0.03 \leqq y \leqq 0.10$.

2. The hetero field effect transistor according to Claim 1, wherein

the composition y satisfies $0.03 \leqq y \leqq 0.07$.

3. The hetero field effect transistor according to Claim 1, wherein

A is As.

4. The hetero field effect transistor according to Claim 1, wherein A is Sb.

5. The hetero field effect transistor according to Claim 1, wherein the channel layer is constituted by only the compound semiconductor layer.

6. The hetero field effect transistor according to Claim 3, wherein the channel layer comprises a first channel layer and a second channel layer which is formed to be adjacent to the first channel layer and hetero-joins to the spacer layer,

the first channel layer is constituted by the compound semiconductor layer, and the second channel layer is constituted by an InAs layer.

7. The hetero field effect transistor according to Claim 6, wherein x is 0.

8. The hetero field effect transistor according to Claim 6, wherein an N concentration in the first channel layer decreases as the N concentration is closer to the second channel layer.

9. The hetero field effect transistor according to Claim 6, wherein a pair of second channel layers are formed to be adjacent to upper and lower surfaces of the first channel layer,

a pair of spacer layers are formed to hetero-join to the pair of second channel layers, respectively, and

a pair of carrier supply layers are formed to be adjacent to the pair of spacer layers, respectively.

10. The hetero field effect transistor according to Claim 6, wherein $0<x$ is satisfied.

11. The hetero field effect transistor according to Claim 10, wherein $3y \leqq x \leqq 0.2$ is satisfied.

12. The hetero field effect transistor according to Claim 10, wherein $0.1 \leqq x \leqq 0.2$ is satisfied.

13. The hetero field effect transistor according to Claim 6, wherein the first channel layer is constituted by a GaInNAs/InAs MQW layer having a multiple quantum well structure formed by alternately stacking a GaInNAs layer constituted by the compound semiconductor layer in which $0<x$ is satisfied and an InAs layer.

14. The hetero field effect transistor according to Claim 6, wherein the first channel layer is constituted by an InNAs/InAs MQW layer having a multiple quantum well structure formed by alternately stacking an InNAs layer constituted by the compound semiconductor layer in which x is 0 and an InAs layer.

15. The hetero field effect transistor according to Claim 1, wherein the buffer layer and the spacer layer are each constituted by an InAlAs layer, and the carrier supply layer is constituted by an n-InAlAs layer.

16. A method of fabricating a hetero field effect transistor, comprising the steps of:

forming a channel layer on a substrate with a buffer layer disposed between the substrate and the channel layer;

forming a spacer layer constituted by a semiconductor having a band gap larger than a band gap of the channel layer to hetero-join to the channel layer; and

forming a carrier supply layer to be adjacent to the spacer layer, wherein

the substrate is made of InP,

the channel layer comprises a compound semiconductor layer represented by a formula $Ga_xIn_{1-x}N_yA_{1-y}$ in which A is As or Sb, composition x satisfies $0 \leqq x \leqq 0.2$, and composition y satisfies $0.03 \leqq y \leqq 0.10$.

17. The method of fabricating a hetero field effect transistor according to Claim 16, wherein ionized N atom is introduced in the step of forming the channel layer.

18. The method of fabricating a hetero field effect transistor according to Claim 16, further comprising the step of:

forming the buffer layer made of InAlAs on the InP substrate, wherein

the step of forming the channel layer comprises the steps of forming a first channel layer made of InNAs on the buffer layer and forming a second channel layer made of InAs on the first channel layer, and

the step of forming the spacer layer comprises the step of forming the spacer layer made of InAlAs on the second channel layer.

19. A transmitter-receiver comprising the hetero field effect transistor according to Claim 1 for processing a transmission signal or a received signal.